dec PERMANENT MEMORANDUM

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SUBJECT DRUM SYSTEM FOR THE PDP-1

TO PDP Distribution List

ABSTRACT This is a discussion of the design and programming aspects of the Magnetic Drum for PDP-1 and is intended to establish these specifications.

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THE DRUM SYSTEM FOR THE PDP-1

The PDP-1 Drum System provides a large backing storage for the magnetic core memory. The drum is ten inches in diameter, twenty inches long, and rotates at 1800 rpm. It has 418 tracks, each with 4,096 bits, giving a storage capacity of greater than 1.6×10^6 bits. Eighteen adjacent tracks form one drum field, 22 fields are stored on the drum. A nineteenth track is used for an odd parity check bit for each field. This parity bit is formed when information is written on the drum, and is checked when information is read from the drum. The drum has a word transfer time of about 8.2 microseconds.

The words on the drum are stored in 4,096 addressable positions. The chief advantage of the PDP-1 Drum System, other than the large storage capabilities, is that simultaneous interchange of core and drum data can take place. Any drum field may transmit to core and any other drum field may receive from core. The address of core and drum may be different.

PROGRAMMING FOR THE DRUM

Several iot orders handle the necessary program selections. Simultaneous drum reading and writing, or reading, or writing, may be effected. A program can specify the function, select the fields of the transfers, the initial addresses of the transfer on the drum, and in core memory, and the number of words to be transfered.

The following orders are used for drum transfers:

iot dia - Set initial drum address:

IO 1 - 5 field written on drum (0 = nothing written on drum, 1 - 22_{10} used)

IO 6 - 17 initial address of drum information

iot dcc - Set count for number of words transferred and initial core address and begin transfer:

IO 1 - 5 field read from drum (0 = nothing written into core memory, 1 - 22 used)

IO 6 - 17 number of words to be transferred

AC 3 - 5 Core memory field information

AC 6 - 17 initial address of core memory information

The transfer begins when dcc is given and all programming, high speed channel transfers, and sequence break action is stopped. The computer returns to location 201 if no parity errors occured in the transfer. A parity error restarts the program location 200.

iot dra - places the current drum address in the IO.

iot pba - transmits a signal (to the Sequence Break System) when the drum position equals the address specified by the IO.